Novel 36 GHz GaAs Frequency Doublers using (M)MIC Coplanar Technology

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Abstract :- The design and performance of single-device and balanced versions of (M)MIC GaAs FET frequency doublers from 18 GHz to 36 GHz, fabricated in purely CPW- techniques are presented. Coplanar discontinuities which are usually neglected are taken into consideration in the analysis and design. Spiral inductors and their assosciated parasitic capacitances are used for impedance matching and phase shifting purposes. Simulation and measurement results are in good agreement. The investigated doublers have a minimum conversion loss of 7 dB.

1. INTRODUCTION

The advantages of coplanar waveguide techniques in the design of (M)MIC circuits have been described elsewhere [1-5]. Among these advantages are the small dispersion of the coplanar line, the ease in realising short circuited ends and the possibility of simple integration of lumped elements or active components. Several GaAs FET frequency doublers in K- and KA-band using microstrips have been reported [6-8]. All of them occupy relatively large space. Few (M)MIC doublers using CPW-techniques operating in K-band have also been reported[2,3,9]. But GaAs FET (M)MIC doublers in KA-band in purely CPW-techniques with the effects of assosciated coplanar discontinuties taken into account is not yet reported. This paper describes the design and realization of different single-device and balanced versions of novel hybrid and monolithic frequency doublers from 18 GHz to 36 GHz in purely coplanar techniques. Moreover, the effects of the unavoidable coplanar discontinuities (such as bends, cross- and T-junctions etc) presented in the circuit, are taken into account in the design. Accurate lumped element equivalent circuit models [4,10] are used to characterize these discontinuities. Simple spiral inductors and their assosciated parasitic capacitances are used for impedance matching and phase shifting purposes. In the balanced doubler version presented here, the conventionally used and space occupying 180-degree hybrid [1,11] is replaced by small size spiral inductors which are carefully designed to give the desired 180-degree phase shift. The doublers are fabricated on ceramic and GaAs substrates. Simulation and measurement results are in good agreement.

2. DESIGN METHOD

The block diagrams of the doublers investigated here are given in Fig. 1. Both the single-device and balanced versions are realized in hybrid and monolithic MIC Technology as described below.

21 The hybrid MIC doublers:

NE710 GaAs FET transistors are mounted in CPW-technique on a ceramic substrate and their S-parameters up to 40 GHz measured. From the measured DC and S-parameters the necessary model parameters of the transistor are extracted. Fig. 2 shows two versions of the hybrid doublers realized. The first one (Version A) called the single-device doubler, uses a symmetrical coplanar band reject stub for harmonic filtering and spiral inductors as matching networks (Fig 2a). The use of symmetrical band-reject helps also to suppress the higher modes [5]. The parasitic capacitances of the spiral inductors are too large to be neglected at the operating frequency and in fact are exploited in the design to serve as part of the matching elements. For the coplanar band reject stub bond wires are necessary to keep the coplanar ground planes on both sides of the cross junction at the same potential (Fig 2a). The problem with the realization of such a circuit is that the resonance frequency is influenced by the length and location of the bond wires used [5] and hence there is a difficulty reproducing the circuit accurately. The second disadvantage is that the stub occupies a relatively large space.

To overcome the above mentioned problems a second type of doubler (Version B) is proposed: namely the push-push or balanced doubler (Fig 2b). This doubler is more compact and has less conversion loss. The balanced doubler proposed here does not utilize the conventionally used [1,11] and space occupying 180°

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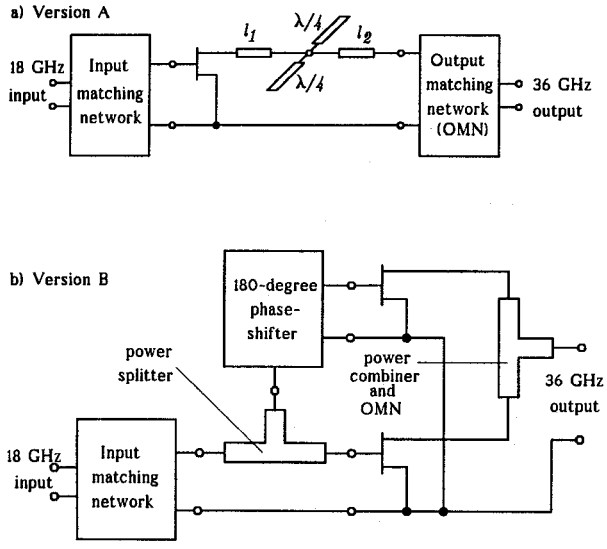

Fig 1 : Block diagrams of the single-device and balanced frequency doublers
a) single-device doubler b) balanced (push-push) doubler

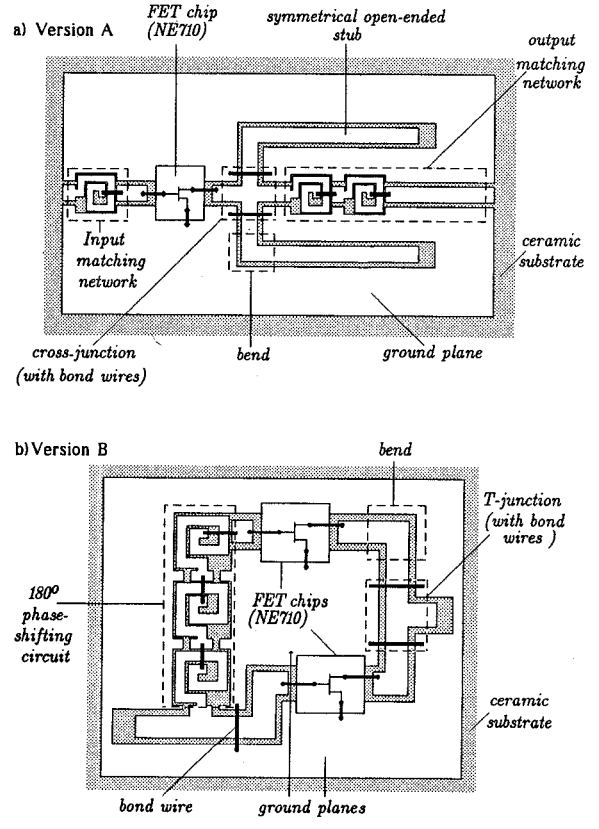

Fig. 2 : Layouts of the 18 to 36 GHz hybrid MIC frequency doublers
a) single-device doubler b) balanced (push-push) doubler

coupler. Instead, simple spiral inductors and their parasitic capacitances are used to obtain the desired 180° phase shift between the gates of the two transistors. The necessary number of spiral inductors and the corresponding windings required for the phase-shifting must be properly optimized. In this way the fundamental frequency at the output will be suppressed and the second harmonic is enhanced. Optimum second harmonic generation is obtained if the transistors are biased near pinch-off (V_g=-0.6V, V_d=1.0V).

2.2 The monolithic MIC doublers:

The advantages of MMIC technology are well known [1,3,9]. Design reproducibility and compactness of the circuit are among its advantages. To this end, the design of the doublers mentioned in section 2.1 are repeated in coplanar MMIC technology on a GaAs substrate (Fig. 3). A 0.3 μm gate length and 200 μm gate width GaAs FET is used for the design. The non-linear model for the transistor is constructed using the Curtice-Ettenberg model . From the measured DC and S-parameters the model parameters are determined. The effects of the assosciated cross- and T-junctions, bends and air bridges are taken into account in the analysis and design. This is done by replacing them with lumped element equivalent circuit models shown in Fig 4 to characterize the coplanar discontinuities [4,10]. One version of the

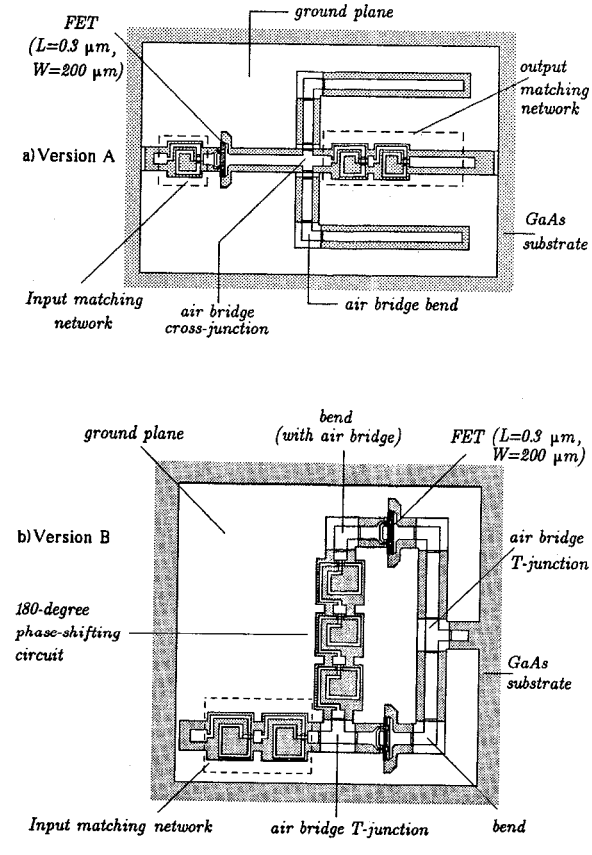

Fig 3: Layouts of the 18 to 36 GHz monolithic MIC frequency doublers
a) single-device doubler b) balanced (push-push) doubler

MMIC balanced doubler including the matching networks occupies a space of 1.5 x 1.5 mm^2. Its layout is shown in Fig 3b.

The monolithic band reject filter at 18 GHz is first fabricated separately and is found to resonate at the desired frequency. The effects of the cross-junction and bends assosciated with this filter are taken into account during the design. Several such filters are fabricated on a GaAs substrate and proved the reproducibility of the design.

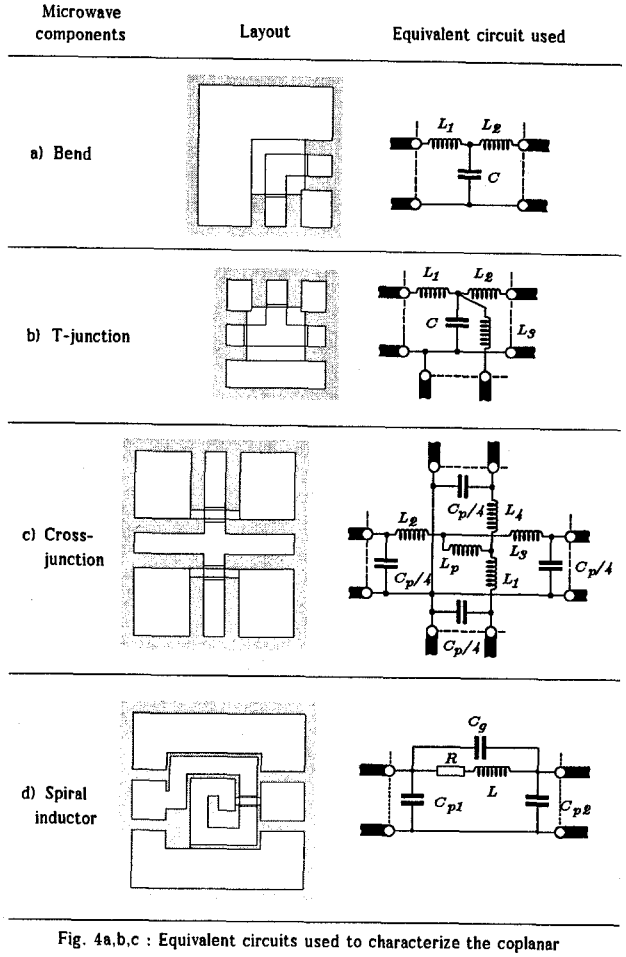

Fig. 4a,b,c : Equivalent circuits used to characterize the coplanar discontinuities
4d : Equivalent circuit of the spiral inductor

3. RESULTS

Fig 5a shows the simulated and measured ouput power (36 GHz) of the single-device hybrid doubler for different input power levels. It shows a minimum conversion loss (C.L) of 10 dB. A 3 dB improvement in the conversion loss (i.e C.L= 7 dB) is achieved if the balanced doubler of Fig 2b is used. Its measured and simulated results are shown in Fig 5b. The single-device and balanced doublers are compared in Fig 6. For the former and the latter the fundamental power

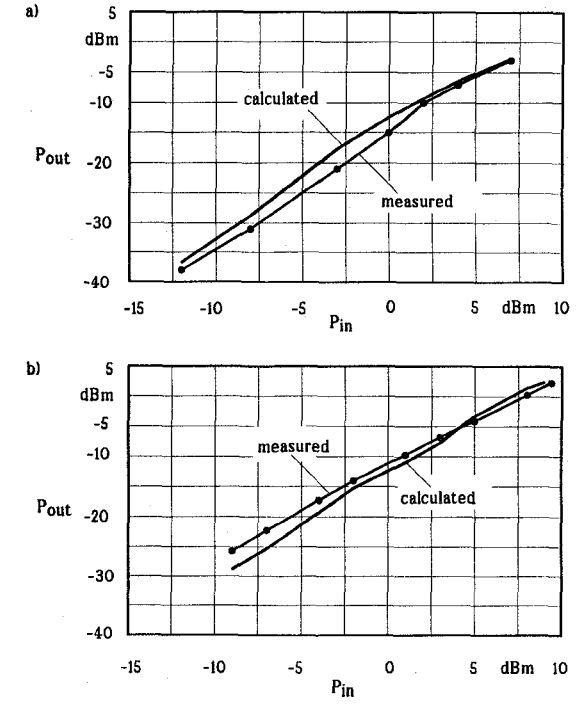

Fig. 5 : Measured and calculated results of the hybrid MIC doublers
a) single-device (Version A) b) balanced (Version B)

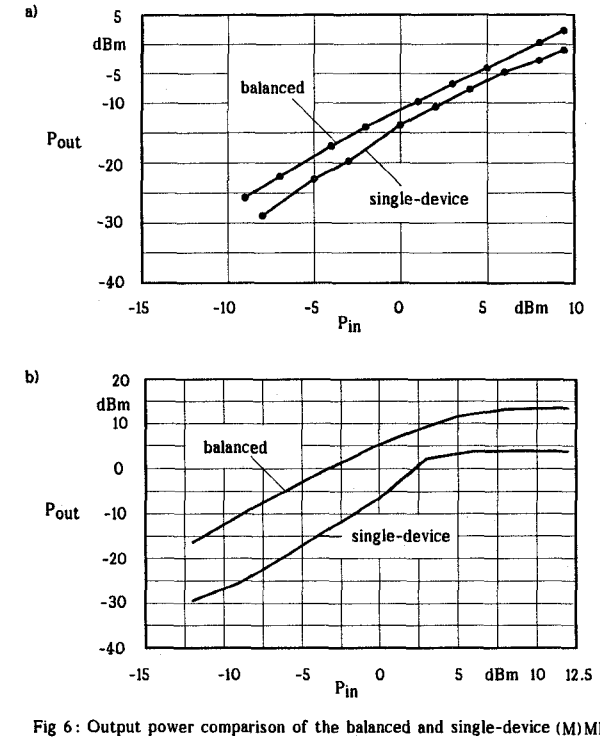

Fig 6: Output power comparison of the balanced and single-device (M)MIC doublers: a) hybrid (measurement) b) monolithic (simulation)

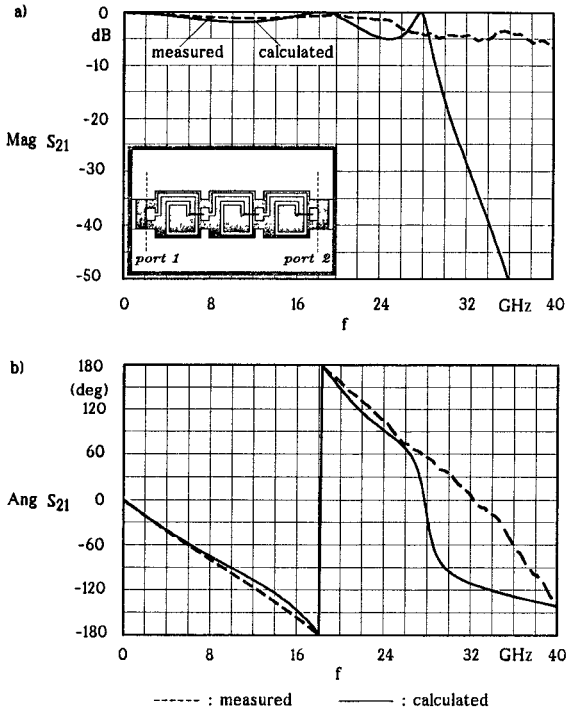

Fig. 7 : Measured and calculated transmission coefficient of the 180° phase-shifting circuit. a) Magnitude b) Phase angle

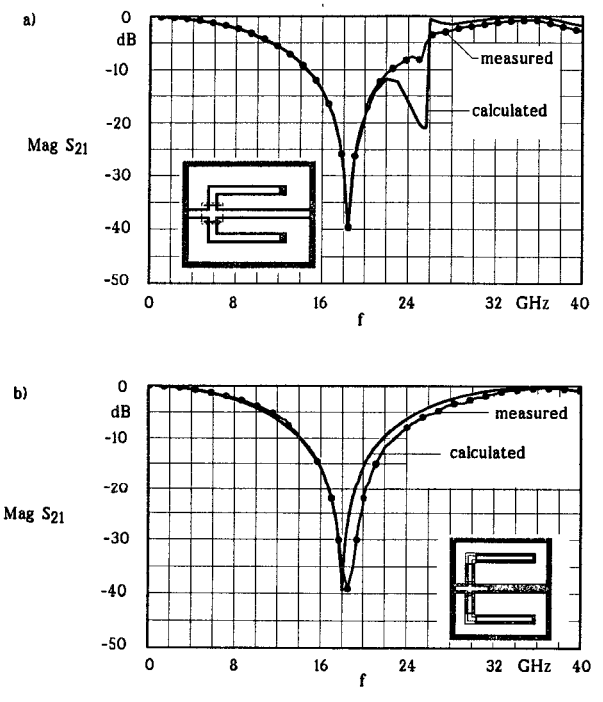

Fig 8 : Measured and calculated rejection levels of the band-reject filters a) hybrid b) monolithic

level lies 15 dB and 19 dB, respectively, below that of the second harmonic power level. The desired 180° phase shifting is successfully achieved by the properly designed spiral inductors. This is demonstrated in Fig 7. Several such 180° phase shifters are fabricated on a ceramic substrate and proved to be reproducible. Fig. 8 shows the measured and calculated transmission coefficients (rejection levels) of both the hybrid and monolithic band-reject filters.

4. CONCLUSIONS

Single-device and balanced frequency doublers in KA-band are designed and fabricated on ceramic and GaAs substrates in purely coplanar (M)MIC Technology. The effects of the coplanar discontinuities are taken into consideration in the design. The calculated and measured results are in good agreement. The doublers have a minimum conversion loss of 7 dB and are small in size, cost-effective and are applicable in small and medium power transmitter/receiver systems.

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